Designing with Siliconix PC Card (PCMCIA) Power Interface Switches

INTRODUCTION

Innovation in portable computer design is driven today by the need for smaller, lighter, and more energy-efficient products. This has been the driving force behind the small form-factor I/O cards that have created an emerging market for PC Cards. In the current version of the PC Card standard, a computer or other "host platform" must be able to deliver some combination of 3.3, 5, and 12 V at the slot for a card to operate. These voltages are then supplied to the card on two supply lines called V_{CC} and V_{PP}.

Vishay Siliconix offers a series of integrated power MOSFETs specifically designed for the strict demands of the PC Card power interface. The, Si9711CY, and Si9712DY devices switch 3.3 V or 5 V to Vcc and 3 V, 5 V, or 12 V to the flash memory program pin, V_{PP} . The Si9706DY and Si9707DY are a functional subset of the Si9712DY. They support only the Vcc line for systems that use V_{PP} from the main supply or future specialized systems that do not support the V_{PP} function.

The Si97XX series of PC Card power interface switches is intended for battery-operated notebook, sub-notebook, and palmtop computers. These monolithic power ICs provide several options for any host platform power switching application. In a single surface-mount package, they provide tighter output tolerances because of their low on-resistance rating, and longer battery life, with leakage currents of less than 1 μA.

PC CARD POWER SWITCHING: AN OVERVIEW

Upon initial card insertion, the PC Card interface must determine its required supply voltages and wake up the card with the proper voltages supplied. The purpose of the PC Card power selector function is therefore that of a power multiplexer, as shown in Figure 1. The switch configuration has been designed for the V_{PP} output to select among all the available voltages (a four-state output), namely 12, 5, and 3.3 V along with ground (0 V). The V_{CC} line is a higher-current three-state output for 5- and 3.3-V circuitry, which also can provide a grounded condition.

VOLTAGE REQUIREMENTS AND REVERSE-BLOCKING CAPABILITY

The power switch requirements in the PC Card voltage selector are unique for at least four reasons. ***First***, the power selector's control interface must follow the PC Card communication format (and interface conveniently to PC Card controller ICs). While the control signals from the interface chip are 3- or 5-V CMOS logic, the 12-V signals must be controlled from this lower voltage input using level shifting. ***Second***, the switches must be bidirectionally blocking since any one of the supplies may go to sleep and short to ground. If the output is held high by another switch, the input is then at a lower potential than the output. One example of this condition is where S1 is off and S2 (as shown in Figure 3 and Figure 4) is on so that V_{PP} is biased to the same potential as V_{CC}. In the event that the 12-V input drops and the supply sleeps, S1 changes from a state where its input voltage exceeds its output to the opposite polarity. Similar cases can occur with S3 and S4.

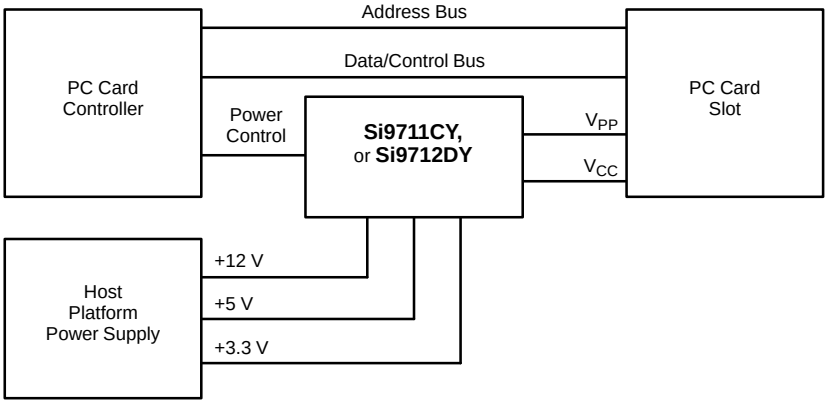

FIGURE 1. Function of Power Selector for PC Cards

LOW ON-RESISTANCE ISSUES

The ***third*** unique aspect of the PC Card voltage selector function is the need for low on-resistance switches, generally below 200 mΩ on the V_{PP} = 12 V switch and even as low as 60 mΩ on the 3.3-V switch. The low on-resistance is not necessarily needed for reasons of power dissipation or high current, but rather to prevent significant voltage drops across the switch. In general, the input to the switch from the system supply may be 4% below nominal, leaving only one percent for the switch. The PC Card standard specifies a maximum variation of ± 5% on both V_{CC} and V_{PP}. This structure is clearly driven by Flash RAM requirements on V_{PP} and the tight rail voltage on 3.3-V ICs. Therefore, the system designer must consider the allowable voltage drop for a maximum expected current on both V_{CC} and V_{PP}. For a 500-mA load at 5 V on V_{CC}, a 1% voltage drop requires a maximum on-resistance of 100 mΩ. The Si9712DY exceeds this requirement over the full temperature range (-40 to 85°C). Assuming a slightly lower current requirement at 3.3 V, the Si9712DY meets 1% voltage drop over the operating temperature range with a maximum specified on-resistance of 80 mΩ.

Because of Vishay Siliconix' pioneering efforts in battery disconnect switches, the PC Card power selector function has been integrated monolithically using the proprietary BCD15 technology. This integrated function actually replaces seven to nine discrete power MOSFETs per slot beyond those involved in the interface and level shifting circuitry.

CONTROLLING THE POWER-UP

The ***fourth*** unique aspect of the PC Card power selector is its need for controlled slew rates on the 3.3-V and 5-V switches. The requisite switching times range from hundreds-of-microseconds to milliseconds: extremely long intervals for integrated circuit technology. Because of the versatility of our BCD15 technology, however, Vishay Siliconix can control the power device behavior over such long intervals.

Designers face a dilemma when dealing with switching ramp times. On the one hand, fast rise times are directly related to the current spikes that can shut down some host platforms. Even the capacitors on PC cards themselves can be damaged by surge currents. Yet some designers correctly wonder whether the ramp time called out by the PC Card Rev. 2.1 standard, as slow as 300 ms, is actually so slow as to latch up and draw excessive current.

The rules in this area are different for different types of host platforms. The small handheld systems that operate off A-cells cannot supply the current to support a fast ramp to a large load. In fact, many of these palmtops attempt to avoid the issue by not offering a Type III slot (although some Type II cards can be categorized as high-power cards). The larger portables have what it takes to supply power to a wider range of cards such as rotating media and the more powerful multimedia or wireless communications cards. For the sake of this discussion, we will group these higher-power systems together as the notebooks.

If a host platform power supply can only handle a certain peak current, then it should control the ramp to support that limit over the range of available cards. Unfortunately, the growing number of card vendors makes the card load a difficult parameter to define without extensive research. According to ongoing surveys of card manufacturers contacted by Vishay Siliconix, this capacitance can be as high as 150 µF. Indeed, cards can be grouped in at least two categories: high-power cards that can have as much as 150-µF bypass on V_{CC}, and low-power cards that are well below a 50-µF bypass on V_{CC}. With these parameters in mind, it is clear from Figure 2 that the host platform with a surge current capability in the milliamp range would need to support a ramp in the low millisecond range for the most reliable operation over the full range of cards.

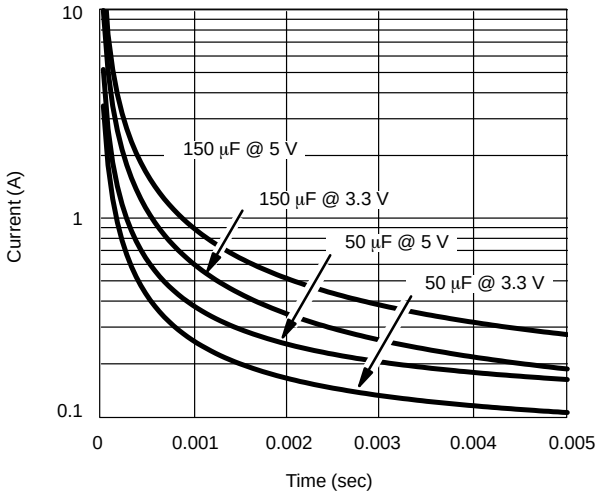

FIGURE 2. Host Platform SOA Curves

The curves in Figure 2 show the safe operating area based on a worst-case assumption of 150-µF card capacitance on V_{CC}. These curves are based on the following calculation:

$$i = C(dv/dt) + I_{steady\ state}$$

where $I_{steady\ state}$ is estimated at 100 mA for 5 V and 70 mA for 3.3 V during the time before the CIS register is read. A 2-ms ramp time is an ideal ramp for a platform that can support a 500-mA surge over the range of card capacitance values. The notebook category of platforms can tolerate a ramp less than 1 ms.

SI9711CY

A host platform design that can support a surge of close to 4 A can comfortably use the Si9711CY, which ramps at 200 µs. However, those systems that cannot tolerate this kind of peak current will be better off with the Si9712DY, which maintains a ramp closer to 1 ms. The Si9706DY and Si9707DY are modelled after the Si9712DY, and therefore support the slower ramp.

PIN DESCRIPTION FOR SI9711CY

S1, S2, S3, S4 (Pins 15, 16, 1, 2)

Control input for selecting appropriate outputs on both V_{CC} and V_{PP}. These four inputs are CMOS compatible and can accommodate 3.3-V and 5-V rails by connecting V_L to the appropriate rail voltage. Each control pin (S1, S2, S3, and S4) individually controls its respective switch (SW1, SW2, SW3, and SW4).

V_L (Pin 14)

This pin is an input to indentify the rail voltage for the control inputs. Connect V_L to the same rail voltage of the PC Card controller for signal voltage compatibility.

+3.3 V_{IN} (Pins 9 and 10)

These pins are the input to provide +3.3 V to the V_{CC} pins of the slot by way of Switch 4, and to V_{PP} by way of Switch 2. Connect these pins to the host platform +3.3-V supply.

+5 V_{IN} (Pin 11)

This pin is the input to provide +5 V to the V_{CC} pins of the slot by way of Switch 3, and to Vpp by way of Switch 2. Connect this pin to the host platform +5-V supply.

+12 V_{IN} (Pin 13)

This pin is the input to provide +12 V to the slot V_{PP} by way of Switch 1. The +12 V_{IN} pin is also used to generate the internal gate drive voltage; therefore, it is important that +12 V is continuous. Connect this pin directly to the host platform +12-V supply. See the section on suspend mode operation for non-continuous 12-V systems.

V_{CC} (Pins 6,7,8,12)

PC Card slot supply voltage. Connect all four pins together and to pins 17 and 51 of the PC Card slot.

Vpp (Pins 4 and 5)

PC Card program and peripheral voltage to slot. Connect both pins together and to pins 18 and 52 of the PC Card slot.

GND (Pin 3)

Ground reference connection. Connect this pin to host platform system ground.

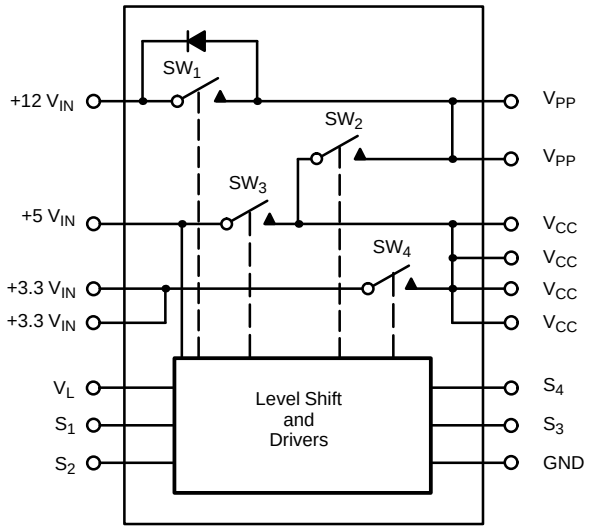

FIGURE 3. Si9711CY Functional Block Diagram

TABLE 1. SI9711CY TRUTH TABLE

S1	S2	S3	S4	V_{PP}	V_{CC}
0	0	0	0	HiZ	HiZ
0	0	0	1	HiZ	3.3 V
0	0	1	0	HiZ	5 V
0	0	1	1	HiZ	Invalid State
0	1	0	0	HiZ	HiZ
0	1	0	1	3.3 V	3.3 V
0	1	1	0	5 V	5 V
0	1	1	1	V_{CC}	Invalid State
1	0	0	0	HiZ	HiZ
1	0	0	1	12 V	3.3 V
1	0	1	0	12 V	5 V
1	0	1	1	12 V	Invalid State
1	1	0	0	Invalid State	HiZ
1	1	0	1	Invalid State	Invalid State
1	1	1	0	Invalid State	Invalid State
1	1	1	1	Invalid State	Invalid State

SI9712DY

The Si9712DY is functionally similar to the Si9711CY with added features. The upgraded configuration of the Si9712DY provides a zero voltage output on V_{CC} and V_{PP}, programmable ramp time on V_{CC}, and meets the PC Card revision 3 PC Card specification scheduled for release in January 1995. Most importantly, it offers better on-resistance in the same package style.

Portable system designers who are interested in maintaining the V_{CC} ± 5% tolerance called out in the PC Card standard will find Si9712DY the best choice. It is designed to support slots intended for “high-power” cards requiring more than an ampere of surge current during normal operation. Some cards that are considered “high-power” cards include rotating media, multimedia, and some wireless communication cards.

The Si9712DY also appeals to the system designer because of the easy interface with the variety of industry-standard controllers. The control inputs for V_{CC} can be configured as active high or active low by simply swapping S3 and S4. Table 2 shows that (1, 1) and (0, 0) on S3, S4 both yield zero out of V_{CC}. Therefore, crossing control lines for SW3 and SW4 will simply change the polarity of the control.

System designers using custom PC Card controllers that are pin constrained may consider tying S2 control high. The Si9712DY truth table (Table 2) shows that S1 will dominate. This limits the operation of the interface by not allowing a state for zero on V_{PP} while V_{CC} is active.

PIN DESCRIPTION FOR THE SI9712DY

S1, S2, S3, S4 (Pins 8, 9, 15, 2)

Control input for selecting appropriate outputs on both V_{CC} and V_{PP}. These four inputs are CMOS compatible and can accommodate 3.3-V and 5-V rails. Each control pin (S1, S2, S3, and S4) individually controls its respective switch (SW1, SW2, SW3, and SW4).

+3.3 V_{IN} (Pins 10 and 11)

These pins are the input to provide +3.3 V to the V_{CC} pins of the slot by way of Switch 4, and to V_{PP} by way of Switch 2. Connect these pins to the host platform +3.3-V supply.

+5 V_{IN} (Pin 12)

This pin is the input to provide +5 V to the V_{CC} pins of the slot by way of Switch 3, and to V_{PP} by way of Switch 2. The +5 V pin is also used to generate the internal gate drive voltage; therefore, it is important that +5 V is continuous. Connect this pin to the host platform +5-V supply. See also the section on advanced sleep modes.

+12 V_{IN} (Pin 14)

This pin is the input to provide +12 V to the V_{PP} of the slot by way of Switch 1. Connect this pin directly to the host platform +12-V supply.

V_{CC} (Pin 5, 6, 7, 13)

PC Card slot supply voltage. Connect all four pins together and to pins 17 and 51.

V_{PP} (Pin 3 and 4)

PC Card program and peripheral voltage to slot. Connect both pins together and to pins 18 and 52.

SR (Pin 16)

Connect a capacitor to the SR pin to adjust the slew rate of the V_{CC} ramp. Recommended capacitance value is identified in the data sheet. This capacitor can be omitted for designs that can tolerate the faster ramp as shown in the Si9712DY data sheet curves.

GND (Pin 1)

Ground reference connection. Connect this pin to the host platform system ground.

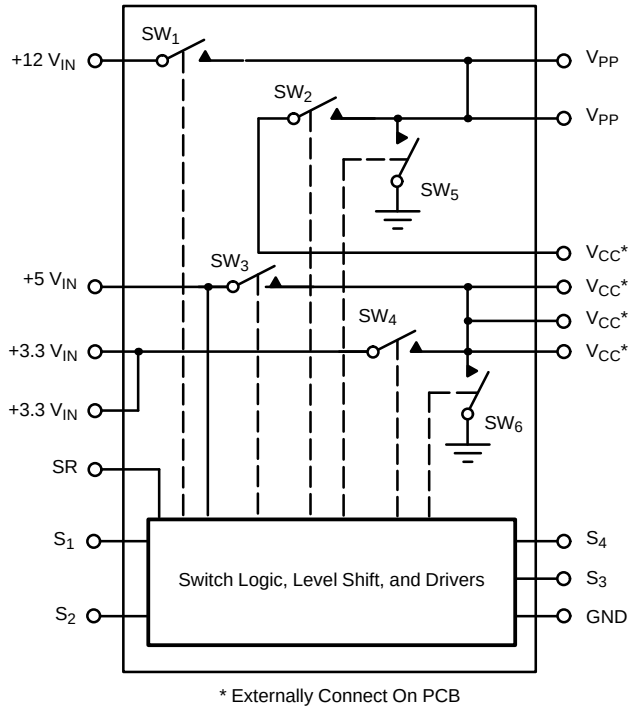

FIGURE 4. Si9712DY Functional Block Diagram

TABLE 2. SI9712DY TRUTH TABLE[a]					
S1	S2	S3	S4	V_{PP} (V)	V_{CC} (V)
0	0	0	0	0	0
0	0	0	1	0	3.3
0	0	1	0	0	5
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	3.3	3.3
0	1	1	0	5	5
0	1	1	1	0	0
1	0	0	0	0	0
1	0	0	1	12	3.3
1	0	1	0	12	5
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	12	3.3
1	1	1	0	12	5
1	1	1	1	0	0

NOTE:
a. Shaded lines are error conditions for P.C. Card applications, however, switches default to the states shown.

SI9706DY AND SI9707DY

The Si9706DY and Si9707DY are interface switches that support only the V_{CC} pins of the PC Card interface. They are intended for systems that support the Vpp programming voltage at the main supply such as the Maxim MAX783 dc-to-dc controller shown in Figure 7.

The Si9706DY is a single V_{CC} power interface switch in an 8-pin SOIC package that switches 3.3 V, 5 V, or 0 V to the V_{CC} pins of the PC Card slot. The Si9707DY is an SO-16 that is equivalent to two Si9706DYs. Both devices have the slow V_{CC} ramptime and smart switching featured in the Si9712DY. The simplified truth table for the Si9706DY and Si9707DY is shown in Table 3.

TABLE 3. SI9706DY/07DY TRUTH TABLE		
S1	S2	V_{CC}
0	0	0 V
0	1	3.3 V
1	0	5 V
1	1	0 V

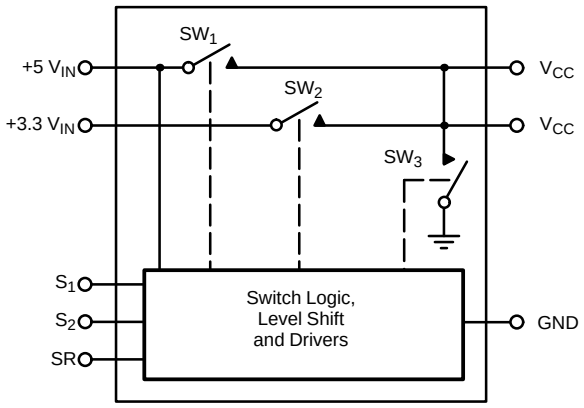

FIGURE 5. Si9706DY Functional Block Diagram

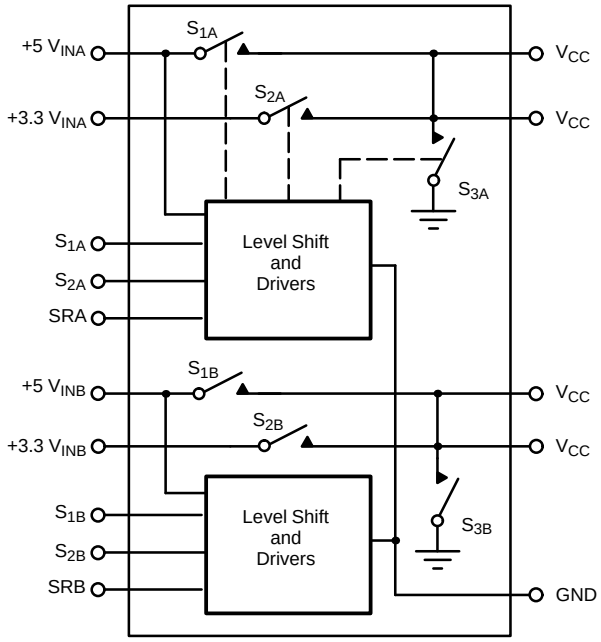

FIGURE 6. Si9707DY Functional Block Diagram

PIN DESCRIPTION FOR THE SI9706DY/9707DY

S1, S2: (Si9706DY: Pin 4, 5) (Si9707DY: Pin 15, 2, 10, 7)

Control input for selecting appropriate outputs on V_{CC}. These two inputs are CMOS compatible and can accommodate 3.3-V and 5-V rails by setting V_L. Table 3 shows V_{CC} output for all states on S1 and S2. For PC Card controllers with active low control signals, S1 and S2 can be reversed.

+3.3 V_{IN}
(Si9706DY: Pin 6) (Si9707DY: Pin 11, 14)

This pin is the input for +3.3 V to be connected to V_{CC} by way of Switch 2. Connect this pin to the host platform +3.3-V supply.

+5 V_{IN}
(Si9706DY: Pin 7) (Si9707DY: Pin 12, 13)

This pin is the input for +5 V to be connected to Vcc by way of Switch 1. Connect this pin to the host platform +5-V supply.

V_{CC}
(Si9706DY: Pin 2, 3) (Si9707DY: Pin 3, 4, 5, 6)

PC Card slot supply voltage. For the Si9706DY, connect pins 2 and 3 of the IC to pins 17 and 51 of the PC card connector. For the Si9707DY, pins 5 and 6 connect to slot A and pins 3 and 4 connect to the slot B pins 17 and 51.

SR
(Si9706DY: Pin 8) (Si9707DY: Pin 9, 16)

Connect a capacitor to the SR pin to adjust the slew rate of the V_{CC} ramp. Recommended capacitance value is identified in the data sheet.

GND
(Si9706DY: Pin 1) (Si9707DY: Pin 8, 1)

Ground reference connection. Connect this pin to host platform system ground.

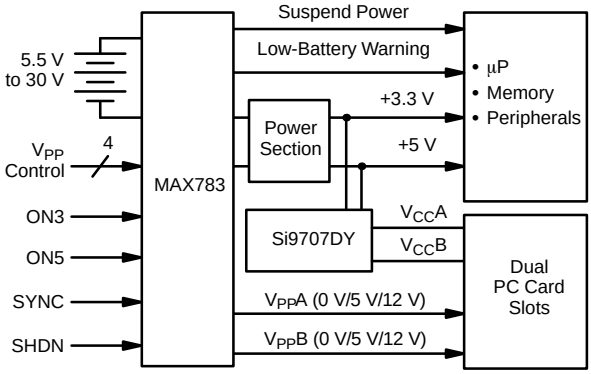

FIGURE 7. Power System Block Diagram Using MAX783 and Si9707DY for Dual PC Card Slots

SLEEP MODE SUPPORT

One of the most common ways of extending battery life is to turn off those supplies which are not being used. Designs that support a power management philosophy that causes +12-V to be intermittent would find the Si9712DY a more suitable part. However, host platforms that turn off the +12-V supply can still use the Si9711CY with the simple external circuit shown in Figure 8.

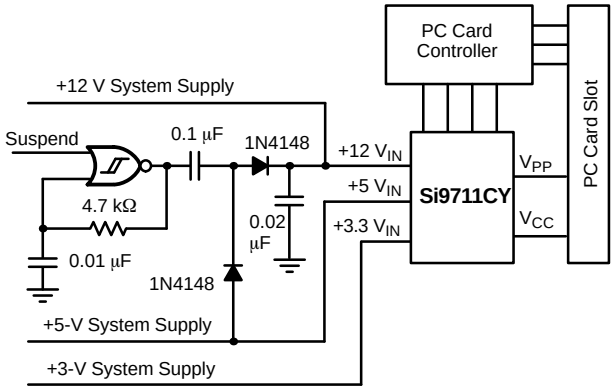

FIGURE 8. Si9711CY Sleep Mode

ADVANCED SLEEP MODE SUPPORT

Today's portable systems have multiple levels of suspend, sleep, or deep-sleep. In certain host platforms, a suspend mode may require maintaining an active slot with the +5-V supply turned off. The best application example for this case is a host platform with a fax/modem card that wakes the system on detecting a ring on the line. This kind of sleep can be done either by using an external circuit similar to the one shown in Figure 8 for suspending +12-V, or by reducing the +5 V_{IN} to 3.3-V. The Si9712DY is functional with no increased on-resistance for card currents below 100 mA (Figure 10).

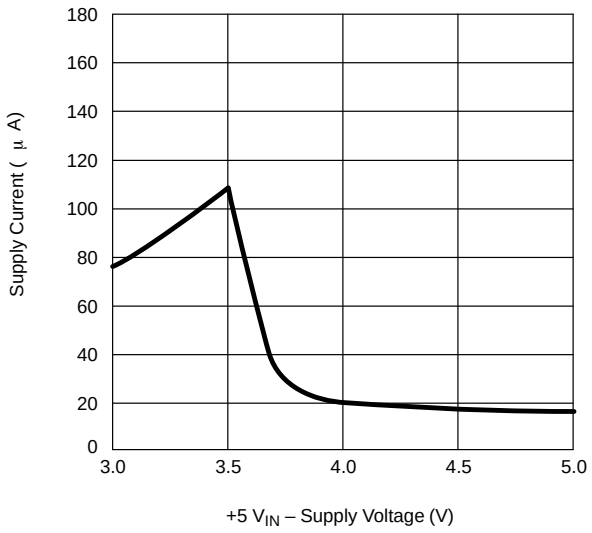

FIGURE 9. Si9712DY Current Draw During Suspend

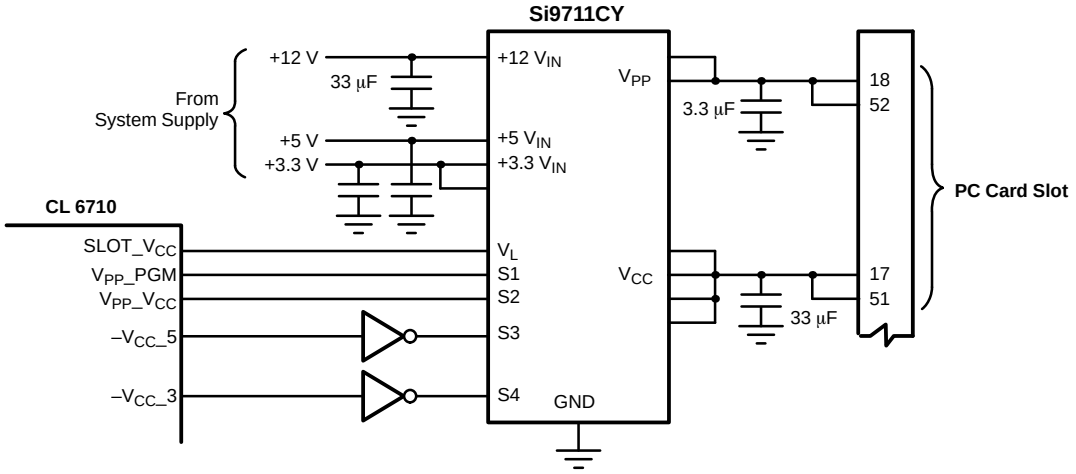

FIGURE 10. Si9711CY System Implementation

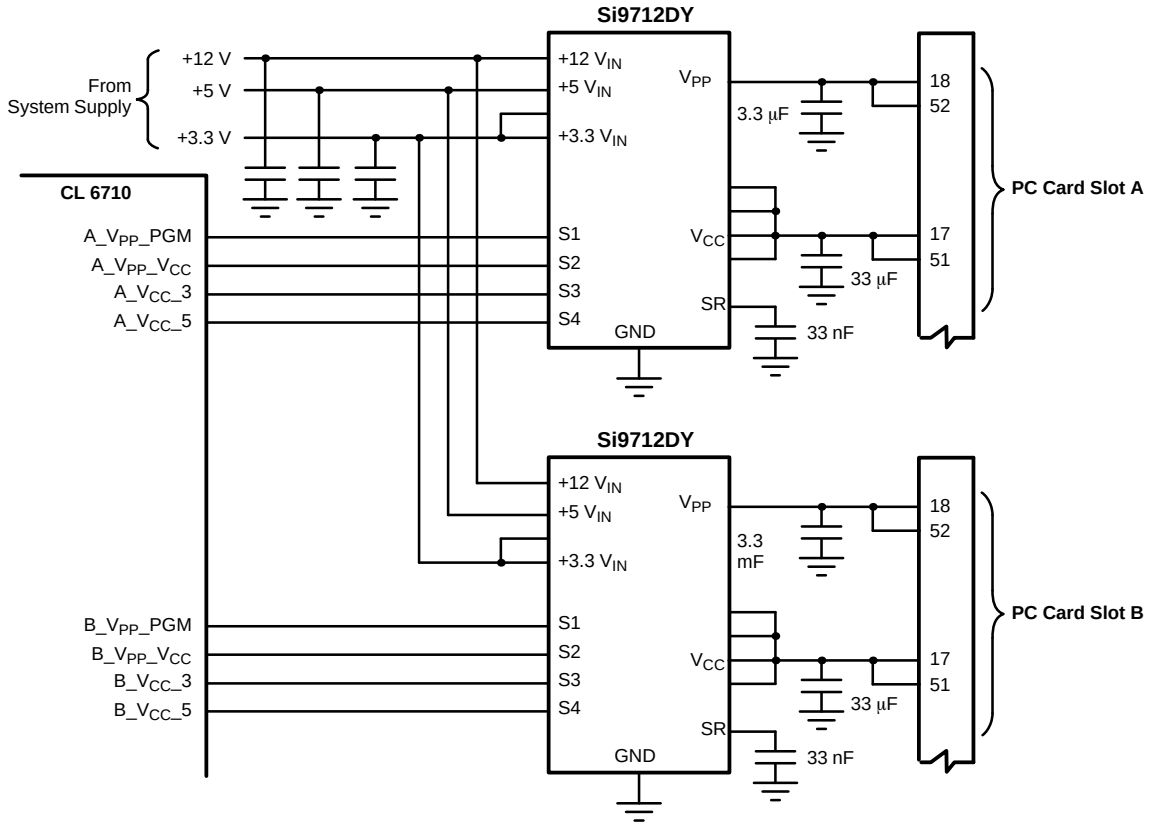

FIGURE 11. Si9712DY System Implementation

CONTROLLER INTERFACE WITH THE SI9711CY

The Si9711CY has individual lines for each switch in the power interface. These control lines can be connected directly to industry-standard controllers that have active high outputs for the switch enables. For controllers that output active low signals for V_{CC} control, such as the Cirrus 6710, the interface would require two inverting buffers as shown in Figure 11. The system power supply, or input side of the switch for 3.3-, 5-, and 12-V should have sufficient bypass capacitance to prohibit switching noise from feeding back into the system supply. For example, the bypass capacitor on +12 V_{in} has been selected as 10 X the bypass on the V_{PP} output pin. Bypass capacitance on the 3.3-V and 5-V inputs will vary based on system implementation and the intended power level that the slot is intended to support. Capacitor values for V_{CC} and V_{PP} are left up to the individual system designer. However V_{CC} should be at least 10 X the capacitance of V_{PP}. They should be selected for optimum ESD protection since these pins interface directly to the PC Card slot.

CONTROLLER INTERFACE WITH THE SI9712DY

The Si9712DY interface supports both active-high and active-low V_{CC} control. The smart switching feature allows the designer to swap the 3.3- and 5-V control to produce an active low interface as shown in Figure 11 with the Cirrus 6720 in a dual-slot configuration.

CONTROLLER INTERFACE WITH THE SI9706DY/07DY

The Si9706DY and Si9707DY interfaces directly to industry-standard PC Card controllers. The Si9707DY would provide the best system choice with the MAX783 dc/dc controller and the Cirrus 6720 dual slot PC Card controller. The Si9706DY and Cirrus 6710 with the MAX783 provide a complete solution for single slot configurations. The Si9706DY and Si9707DY support active high and active low control signals in the same way as Si9712DY.